What Is Claimed Is:

1. A liquid crystal display device, comprising:

a plurality of gate lines extended from each gate on a substrate;

a gate insulating layer on the substrate including the gate lines;

a plurality of data lines arranged to be perpendicular to the gate lines;

a passivation layer over the data lines and the gate insulation layer;

a plurality of etching holes in the passivation layer and the gate insulating layer, wherein the gate insulating layer within the etching holes has at least one concave and convex portions; and

a plurality of seal pattern lines in the etching holes.

2. The liquid crystal display according to claim 1, wherein the gate insulation layer includes an inorganic material.

3. The liquid crystal display according to claim 2, wherein the inorganic material is selected from the group consisting of at least one of silicon oxide and silicon nitride.

4. The liquid crystal display according to claim 1, wherein the etching hole has one of a circular, quadrilateral, straight line, and lattice shapes.

5. The liquid crystal display according to claim 1, wherein the passivation layer includes an organic material.

6. The liquid crystal display according to claim 5, wherein the organic material is selected from the group consisting of at least one of benzocyclobutene and acryl.

7. The liquid crystal display according to claim 1, wherein the passivation layer within the etching holes substantially matches the convex portion of the gate insulating layer.

8. A liquid crystal display device, comprising:

a plurality of gate lines extended from each gate on a substrate;

a gate insulating layer on the substrate including the gate lines;

a plurality of data lines arranged to be perpendicular to the gate lines;

a passivation layer over the data lines and the gate insulation layer;

a plurality of etching holes in the passivation layer and the gate insulating layer, wherein the gate insulating layer within the etching holes has at least one concave and convex portions and the passivation layer within the etching holes substantially matches the convex portion of the gate insulating layer;

a plurality of seal pattern lines in the etching holes; and

an adhesion enhancing metal line between the substrate and the seal pattern lines.

9. The liquid crystal display according to claim 8, wherein the adhesion enhancing metal line directly contacts the substrate and the seal pattern lines.

10. The liquid crystal display according to claim 8, wherein the adhesion enhancing metal line directly contacts the gate insulating layer and the seal pattern lines.

11. A method of fabricating a liquid crystal display device, the method comprising:

forming a plurality of gate lines extended from each gate on a substrate;

forming a gate insulating layer on the substrate including the gate lines;

forming a plurality of data lines arranged to be perpendicular to the gate lines;

forming a passivation layer over the data lines and the gate insulation layer;

forming a plurality of etching holes in the passivation layer and the gate insulating layer, wherein the gate insulating layer within the etching holes has at least one concave and convex portions; and

forming a plurality of seal pattern lines in the etching holes.

12. The method according to claim 11, wherein the step of forming a plurality of etching holes in the passivation layer and the gate insulating layer includes:

forming a photoresist layer on the passivation layer;

exposing a portion of the photoresist layer using a mask having slits;

stripping the exposed portion of the photoresist layer using a stripping solution, thereby forming an at least one concave and convex portions on the surface of the photoresist layer; and

removing a portion of the passivation layer and the gate insulating layer to form a plurality of etching holes.

13. The method according to claim 11, wherein the step

of forming a plurality of etching holes in the passivation layer and the gate insulating layer includes the steps of:

forming a photoresist layer on the passivation layer;

patterning the photoresist layer to have patterns; and

removing a portion of the passivation layer and the gate insulating layer to form a plurality of etching holes, wherein the etching holes substantially match the patterns of the photoresist layer.

14. A method of fabricating a liquid crystal display device, the method comprising:

forming a plurality of gate lines extended from each gate on a substrate;

forming a gate insulating layer on the substrate including the gate lines;

forming a plurality of data lines arranged to be perpendicular to the gate lines;

forming a passivation layer over the data lines and the gate insulation layer;

forming a plurality of etching holes in the passivation layer and the gate insulating layer, wherein the gate insulating layer within the etching holes has at least one concave and convex portions and the passivation layer within the etching holes substantially matches the convex portion of the gate insulating layer;

forming a plurality of seal pattern lines in the etching holes; and

forming an adhesion enhancing metal line between the substrate and the seal pattern lines.

15. The method according to claim 14, wherein the adhesion enhancing metal line directly contacts the substrate and the seal pattern lines.

16. The method according to claim 14, wherein the adhesion enhancing metal line directly contacts the gate insulating layer and the seal pattern lines.

17. An array substrate for a liquid crystal display device, comprising:

a plurality of gate lines arranged in a transverse direction on a substrate;

a plurality of data lines arranged in a longitudinal direction perpendicular to each gate line;

a plurality of switching elements, each switching element includes,

a gate electrode extended from the gate line;

a source electrode extended from the data line;

a drain electrode space apart from the source electrode;

a gate insulation layer on the gate electrode; and

an active layer interposed between the gate insulation layer and the source and drain electrodes;

a passivation layer over the switching elements and on the gate insulation layer, the passivation layer having a drain contact hole to the drain electrode;

a pixel electrode corresponding to each switching element, the pixel electrode contacting the drain electrode through the drain contact hole; and

a plurality of seal pattern lines that are arranged along edges of the passivation layer;

wherein each seal pattern line is disposed in a seal pattern area that has a width over the substrate;

wherein the seal pattern area is defined along the edges of the passivation layer; and

wherein the seal pattern area has a plurality of internal indentations and external projection.

18. The array substrate according to claim 17, wherein the internal indentations are formed between the data lines in the seal pattern area.

19. The array substrate according to claim 17, wherein each internal indentation has at least one of circular, quadrilateral, lattice, and longitudinal lines.

20. The array substrate according to claim 17, further comprising an adhesion enhancing metal layer below the seal pattern area.

21. The array substrate according to claim 20, wherein some portions of the adhesion enhancing metal layer are exposed by a plurality of the internal indentations.

22. The array substrate according to claim 20, wherein the adhesion enhancing metal layer and the plurality of the gate lines are formed at the same time.

23. The array substrate according to claim 20, wherein the adhesion enhancing metal layer and the plurality of the data lines are formed at the same time.

24. A method of forming a seal pattern for a liquid crystal display device, the method comprising:

forming a plurality of gate lines in a transverse direction on a substrate;

forming a plurality of gate electrodes, each gate electrodes extended from each gate line;

forming a gate insulation layer on the substrate to cover the gate lines and the gate electrodes;

forming an active layer on the gate insulation layer and over each gate electrode;

forming a plurality of data lines on the gate insulation layer, each data lines is perpendicular to the gate lines;

forming source and drain electrodes on the active layer and over each gate electrode, source and drain electrodes spaced apart from each other;

forming a passivation layer on the gate insulation layer to cover the data lines and the source and drain electrodes;

defining a seal pattern area on a surface of the passivation layer and along edges of the passivation layer, the seal pattern area having a width; and

etching portions of the passivation and gate insulation layers which correspond to the seal pattern area to form a plurality of internal indentation and external projection.

25. The method of forming the seal pattern according to claim 24, further comprising the step of forming an adhesion enhancing metal layer on the substrate and below the seal pattern area at the same time as the step of forming a plurality of the gate lines.

26. The method of forming the seal pattern according to claim 24, further comprising the step of forming an adhesion enhancing metal layer on the gate insulation layer and below

the seal pattern area at the same time as the step of forming a plurality of the data lines.

27. The method of forming the seal pattern according to claim 24, wherein each internal indentation has at least one of circular, quadrilateral, lattice, and longitudinal line shape.

28. The array substrate according to claim 17, wherein the internal indentations are formed between the gate lines in the seal pattern area.